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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete If Known	
				Application Number	10/066,095
				Filing Date	1/31/2002
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	Brandon Bowers
Sheet	1	of	1	Attorney Docket Number	SPLX.P0074

FOREIGN PATENT DOCUMENTS								
Examiner's Initials	Cite No. ¹	Foreign Patent Document			Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ²	Number ³	Kind Code (if known) ⁵				
BB	1.	JP	02-262354		10-25-1990	Kuribayashi, Mototaka		

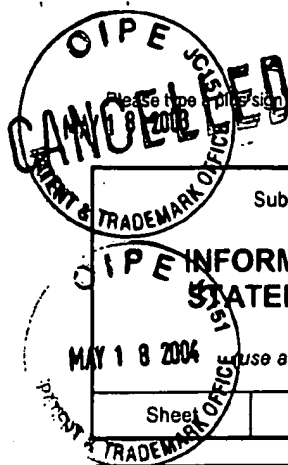
NON PATENT LITERATURE DOCUMENTS								
Examiner's Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.						T ⁶
BB	2.	CHO J.D., Wiring Space and Length Estimation in Two-Dimensional Arrays, May 2000, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, VOL. 19, Iss. 5, pp. 612-615.						
BB	3.	CONG J. et al., DUNE - A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.						
BB	4.	DION J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95-3, pp. 1-22.						
BB	5.	JUTTNER et al., "Lagrange Relaxation Based Method for the QoS Routing Problem, IEEE, Apr. 26, 2001, pp 259-268.						
BB	6.	SCHULZ U., Hierarchical Physical Design System, CompEuro '89, VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks. Proceedings, 8-12 May 1989, pp. 5/20 - 5/24.						
BB	7.	TSENG H-P. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.						

Examiner Signature		Date Considered	12/13/04
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OIPE INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	1/31/2002
Use as many sheets as necessary)				First Named Inventor	Steven Teig et al.
				Group Art Unit	3628-2825
				Examiner Name	Chenevski, S. Bowers
Sheet	1	of	9	Attorney Docket Number	SPLX.P0074

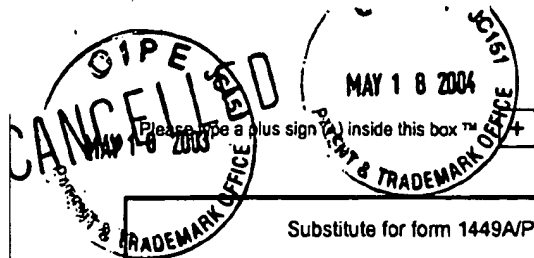
U.S. PATENT APPLICATIONS						
Examiner Initials	Cite No. ¹	U.S. Patent Application		Name of Patentee or Applicant of Cited Document	Date of Filing MM-DD-YYYY	Related Application Data if any
		Serial Number	Attorney Docket Number			
BB	1.	10/066,060	SPLX.P0072	Steven Teig	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	2.	10/066,160	SPLX.P0073	Steven Teig	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	3.	10/066,047	SPLX.P0078	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	4.	10/061,641	SPLX.P0079	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	5.	10/066,094	SPLX.P0080	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	6.	10/076,121	SPLX.P0081	Steven Teig et al.	02-12-2002	CIP of 10/066,094.
MB	7.	10/062,995	SPLX.P0105	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	8.	10/066,102	SPLX.P0106	Steven Teig	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
MB	9.	10/066,187	SPLX.P0133	Steven Teig et al.	01-31-2002	Application filed on the same date, with same specification and drawings, but with different summary and abstract.
BB	10.	10/286,584	CDN.P0037	Steven Teig	10-31-2002	
BB	11.	10/335,087	CDN.P0038	Steven Teig et al.	12-31-2002	
BB	12.	10/335,239	CDN.P0039	Steven Teig et al.	12-31-2002	

Examiner Signature	<i>Anthony Bowers</i>	Date Considered	12/13/04
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				Filing Date	1/31/2002
				First Named Inventor	Steven Teig et al.
				Group Art Unit	3628 2825
				Examiner Name	Chencinski, S. Bowers
Sheet	2	of	9	Attorney Docket Number	SPLX.P0074
U.S. PATENT APPLICATIONS					
	13.	10/335,086	CDN.P0040	Steven Teig et al.	12-31-2002

FOREIGN PATENT DOCUMENTS								
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		Office ³	Number ⁴	Kind Code (if known) ⁵				
	14.	JP	11-296560		10-29-1999	Matsumoto et al.	with English translation of Abstract;	
BB	15.	JP	2000-082743		03-21-2000	Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
BB	16.	JP	64-15947		01-19-1989	Ouchi	with English translation of Abstract;	
BB	17.	JP	03-173471		07-26-1991	Tawada et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
BB	18.	JP	04-000677		01-06-1992	Fujiwara et al.	with English translation of Abstract;	
BB	19.	JP	05-102305		04-23-1993	Sato	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
BB	20.	JP	05-243379		09-21-1993	Kubota	with Japanese Patent Office's English translation of Abstract;	✓

Examiner Signature	Brian Bower	Date Considered	12/13/04
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

MAY 18 2004

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Sheet

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of

9

Application Number

10/066,095

Filing Date

1/31/2002

First Named Inventor

Steven Teig et al.

Group Art Unit

3628

2825

Examiner Name

Chencinski, S. Bomer

Attorney Docket Number

SPLX.P0074

FOREIGN PATENT DOCUMENTS

							and with English translation of the application.	
BB	21.	JP	07-086407		03-31-1995	Miura	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
BB	22.	JP	09-162279		06-20-1997	Yoshida	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓

NON PATENT LITERATURE DOCUMENTS

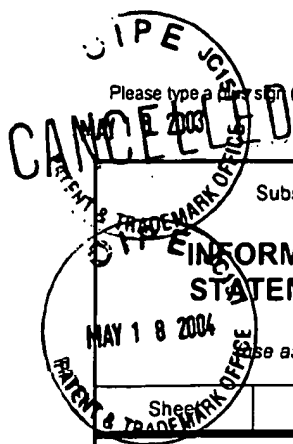
Examiner's Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
BB	23.	Chen, H.F. et al., A Faster Algorithm for Rubber-Band Equivalent Transformation for Planar VLSI Layouts, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 15, No. 2, February 1996, pp. 217-227.	
BB	24.	Chip Model with Wiring Cost Map, August 1983, IBM Technical Disclosure Bulletin, vol. 26, issu. 3A, pp. 929-933	
BB	25.	Dayan, T. et al., Layer Assignment for Rubber Band Routing, UCSC-CRI-93-04, January 20, 1993.	
BB	26.	Dayan, T., Rubber-Band Based Topological Router, A Dissertation, UC Santa Cruz, June 1997.	
BB	27.	Dood, P. et al. A Two-Dimensional Topological Compactor with Octagonal Geometry, 28 th ACM/IEEE Design Automation Conference, pp 727-731, July 1991.	

Examiner Signature		Date Considered	12/17/04
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Sheet

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Application Number	10/066,095
Filing Date	1/31/2002
First Named Inventor	Steven Teig et al.
Group Art Unit	3620-2328
Examiner Name	Chencinski, S. Powers
Attorney Docket Number	SPLX.P0074

NON PATENT LITERATURE DOCUMENTS

BB	28.	Fujimura, K. et al, Homotopic Shape Deformation.	
BB	29.	Hama, T. et al., Curvilinear Detailed Routing Algorithm and its Extension to Wire-Spreading and Wire-Fattening.	
BB	30.	Hama, T. et al., Topological Routing Path Search Algorithm with Incremental Routability Test, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, No. 2, February 1999, pp. 142-150.	
BB	31.	Kobayashi, K. et al., A New Interactive Analog Layout Methodology based on Rubber-Band Routing, UCSC-CRL-96-12, June 13, 1996.	
BB	32.	Lim, A. et al, A Fast Algorithm To Test Planar Topological Routability, Technical Report 94-012, pp. 1-16.	
BB	33.	Lu, Y., Dynamic Constrained Delaunay Triangulation and Application to Multichip Module Layout, A Thesis for Master of Science, UC Santa Cruz, December 1991.	
BB	34.	Maley, F.M., Testing Homotopic Routability Under Polygonal Wiring Rules, Algorithmica 1996, 15: 1-16.	
BB	35.	Morton, P. B. et al., An Efficient Sequential Quadratic Programming Formulation of Optimal Wire Spacing for Cross-Talk Noise Avoidance Routing, UCSC-CRL-99-05, March 10, 1999.	
BB	36.	NN71091316, Use of Relatively Diagonal And Rectangular Wiring Planes n Multilayer Packages, September 1971, IBM Technical Disclosure Bulletin, Vol. No. 14, Issue No. 4, pp. 1316-1317.	
BB	37.	Staepelaere, D. et al., Geometric Transformations for a Rubber-Band Sketch, A Thesis for a Master of Science in Computer Engineering, UCSC, September 1992.	
BB	38.	Staepelaere, D. et al., Surf: A Rubber-Band Routing System for Multichip Modules, pp 18-26, 1993.	
BB	39.	Su, J. et al., Post-Route Optimization for Improved Yield Using Rubber-Band Wiring Model, 1997 International Conference on Computer-Aided Design, pp 700-706, November 1997.	
BB	40.	Wei-Ming Dai, W. et al., Routability of a Rubber-Band Sketch. 28 th ACM-IEEE Design Automation Conference, 1991. pp. 45-65.	
BB	41.	Xing, Z. et al., A Minimum Cost Path Search Algorithm Through Tile Obstacles, slide presentation.	
BB	42.	Xing, Z. et al., Shortest Path Search Using Tiles and Piecewise Linear Cost Propagation, IEEE, 2002, pp.145-158.	

Examiner Signature	<i>[Signature]</i>	Date Considered	12/13/04
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			First Named Inventor	Steven Teig et al.	
			Group Art Unit	3628 2826	
			Examiner Name	Chencinski, S. <i>Bowen</i>	
Sheet	5	of	9	Attorney Docket Number	SPLX.P0074

NON PATENT LITERATURE DOCUMENTS

<i>BB</i> ✓	43.	Xu, A More Efficient Distance Vector Routing Algorithm, UCSC-CRL-96-18, March 1997.	
<i>BB</i> ✓	44.	Yu, M.-F. et al., Fast and Incremental Routability Check of a Topological Routing Using a Cut-Based Encoding, UCSC-CRL-97-07, April 14, 1997.	
<i>BB</i> ✓	45.	Yu, M.-F. et al, Interchangeable Pin Routing with Application to Package Layout, UCSC-CRL-96-10, April 25, 1996.	
<i>BB</i> ✓	46.	Yu, M.-F. et al., Pin Assignment and Routing on a Single-Layer Pin Grid Array, UCSC-CRL-95-15, February 24, 1995.	
<i>BB</i> ✓	47.	Yu, M.-F. et al., Planar Interchangeable 2-Terminal Routing, UCSC-CRL-95-49, October 19, 1995.	
<i>BB</i> ✓	48.	Yu, M.-F. et al., Single-Layer Fanout Routing and Routability Analysis for Ball Grid Arrays, UCSC-CRL-95-18, April 25, 1995.	
<i>BB</i> ✓	49.	Ahuja, R. et al., Faster Algorithms for the Shortest Path Problem, Journal of the Association for Computing Machinery, vol. 37, No. 2, April 1990, pp. 213-223.	
<i>BB</i> ✓	50.	Alexander, M. et al., Performance-Oriented Placement and Routing for field-programmable gate arrays, Proceedings of the European Design Automation Conference, pages 80-85, 1995.	
<i>BB</i> ✓	51.	Alexander, M. et al., Placement and Routing for Performance-Oriented FPGA Layout, VLSI Design, Vol. 7, No. 1, 1998.	
<i>BB</i> ✓	52.	Andou, H. et al., Automatic Routing Algorithm for VLSI, 22 nd Design Automation Conference, 1985, pp. 785-788.	
<i>BB</i> ✓	53.	Bagga, J. et al., Internal, External, and Mixed Visibility Edges of Polygons.	
<i>BB</i> ✓	54.	Berger, B. et al., Nearly Optimal Algorithms and Bounds for Multilayer Channel Routing, Journal of the Association for Computing Machinery, pp. 500-542, March 1995.	
<i>BB</i> ✓	55.	Brady, L. et al., Channel Routing on a 60° Grid, extended abstract, pp.926-931.	
<i>BB</i> ✓	56.	Carothers, K., A Method of Measuring Nets Routability for MCM's General Area Routing Problems, 1999, pp. 186-192.	
<i>BB</i> ✓	57.	Chen, D-S. et al., A Wire-Length Minimization Algorithm for Single-Layer Layouts	

Examiner Signature	<i>Bowen Bowen</i>	Date Considered	12/13/04
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First Named Inventor

Steven Teig et al.

Group Art Unit

3628

2826

Examiner Name

Chencinski, S.

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Attorney Docket Number

SPLX.P0074

NON PATENT LITERATURE DOCUMENTS

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of

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Application Number	10/066,095
Filing Date	1/31/2002
First Named Inventor	Steven Teig et al.
Group Art Unit	3628 2825
Examiner Name	Chencinski, S. <i>Bower</i>
Attorney Docket Number	SPLX.P0074

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Examiner Signature	<i>Arthur Bower</i>	Date Considered	12/13/04
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Application Number	10/066,095
Filing Date	1/31/2002
First Named Inventor	Steven Teig et al.
Group Art Unit	9628 2828
Examiner Name	Chencinski, S. J. Sawyer
Attorney Docket Number	SPLX.P0074

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Sheet 8 of 9

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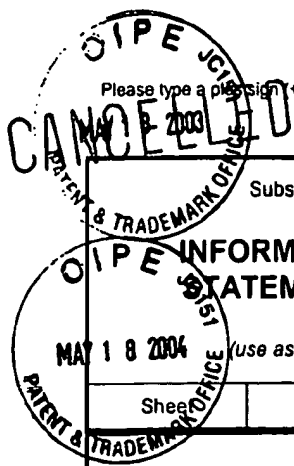
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Application Number

10/066,095

Filing Date

1/31/2002

First Named Inventor

Steven Teig et al.

Group Art Unit

~~3028~~ 2826

Examiner Name

Ghencincki, S. *Bower*

Attorney Docket Number

SPLX.P0074

NON PATENT LITERATURE DOCUMENTS

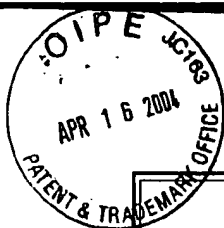
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Title of Invention	Method and apparatus for routing groups of paths																																																														
<p>Application Number: 10/066095</p> <p>Confirmation Number: 6009</p> <p>First Named Applicant: Steven Teig</p> <p>Attorney Docket Number: SPLX.P0074</p> <p>Art Unit: 3628 2825</p> <p>Examiner: SIEGFRIED E. CHENCINSKI <i>Baner</i></p> <p>Search string: (4615011 or 4782193 or 5633479 or 5634093 or 5635736 or 6128767 or 6219823 or 6226560 or 6262487 or 6295634 or 6436804 or 6490713 or 6546540 or 6645842 or 4673966 or 4855929 or 5360948 or 5375069 or 5532934 or 5578840 or 5618744 or 5636125 or 5637920 or 5650653 or 5657242 or 5659484 or 5663891 or 5717600 or 5723908 or 5742086 or 5757089 or 5757656 or 5777360 or 5811863 or 5822214 or 5838583 or 5859449 or 5889329 or 5889677 or 5898597 or 5914887 or 5973376 or 5980093 or 6035108 or 6038383 or 6058254 or 6067409 or 6068662 or 6088519 or 6111756 or 20020104061 or 20020100009 or 20020107711 or 20020182844 or 20030005399 or 20030188281 or 20010003843 or 20020174413 or 20030025205 or 20030121017).pn.</p> <p>US Patent Documents</p> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td><i>04</i></td><td>1</td><td>4615011</td><td>1986-09-30</td><td>Linsker</td><td></td><td></td><td></td></tr><tr><td><i>04</i></td><td>2</td><td>4782193</td><td>1988-11-01</td><td>Linsker</td><td></td><td></td><td></td></tr><tr><td><i>04</i></td><td>3</td><td>5633479</td><td>1997-05-27</td><td>Hirano</td><td></td><td></td><td></td></tr><tr><td><i>04</i></td><td>4</td><td>5634093</td><td>1997-05-27</td><td>Ashida et al.</td><td></td><td></td><td></td></tr><tr><td><i>04</i></td><td>5</td><td>5635736</td><td>1997-06-03</td><td>Funaki et al.</td><td></td><td></td><td></td></tr><tr><td><i>04</i></td><td>6</td><td>6128767</td><td>2000-10-03</td><td>Chapman</td><td></td><td></td><td></td></tr></tbody></table>								init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	<i>04</i>	1	4615011	1986-09-30	Linsker				<i>04</i>	2	4782193	1988-11-01	Linsker				<i>04</i>	3	5633479	1997-05-27	Hirano				<i>04</i>	4	5634093	1997-05-27	Ashida et al.				<i>04</i>	5	5635736	1997-06-03	Funaki et al.				<i>04</i>	6	6128767	2000-10-03	Chapman			
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Robert Brown

12/13/04

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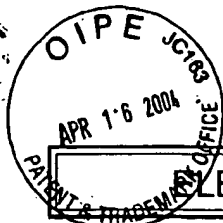
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✓	10	20030121017	2003-06-26	Andreev et al.	A1		

Signature

Examiner Name	Date
<i>Barbara Brown</i>	12/13/04



ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	Method and apparatus for routing groups of paths
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Application Number: 10/066095



Confirmation Number: 6009

First Named Applicant: Steven Teig

Attorney Docket Number: SPLX.P0074

Art Unit:

~~2028~~ 2326

Examiner:

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Search string:

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or 6209123 or 6216252 or 6219832 or 6230306
or 6247167 or 6253363 or 6260179 or 6289495
or 6292929 or 6301686 or 6324674 or 6324675
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or 6412097 or 6412102 or 6463575 or 6473891
or 6519751 or 6526555 or 6543043 or 6557145
or 6567967 or 6586281 or 6665852).pn.

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
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